What is claimed is:

1. A solid-state imaging device comprising:

unit pixels including as constituent elements

a charge generating section for generating a signal charge in an amount corresponding to a light received,

a charge storing part for storing a charge generated by the charge generating section,

a transfer gate section arranged between the charge generating section and the charge storing part and for transferring the signal charge generated by the charge generating section to the charge storing part,

a pixel signal generating section for generating a pixel signal commensurate with the signal charge stored in the charge storing part, and

a reset section for resetting the signal charge at the charge storing part;

a transfer line connected commonly with other unit pixels and connected to the transfer gate section;

a transfer drive buffer for driving the transfer line;

a reset line connected commonly with other unit pixels and connected to the reset section;

a reset drive buffer for driving the reset line;

a drain line connected commonly with other unit pixels and connected to the reset section and the pixel signal generating section;

a drain drive buffer for driving the drain line; and

a signal line for receiving the pixel signal generated by the pixel signal generating section and connected commonly with other unit pixels;

whereby a pixel select operation, for outputting the pixel signal generated by the pixel signal generating section onto the signal line, is carried out under potential control at the charge storing part; and

an off transition time, on a voltage waveform on the drain line to be driven by the drain drive buffer of upon applying a drive pulse to the drain drive buffer, is five times or greater and ten thousand times or smaller relative to an off transition time on any of the reset line to be driven by the reset drive buffer and the transfer line to be driven by the transfer driven buffer.

2. A solid-state imaging device according to claim 1, wherein the off transition time on the drain line is in a range of 50 to 600 times relative to an off transition time on any of the reset line and the transfer line.

3. A solid-state imaging device according to claim 1, further comprising a pixel region arranged with the unit pixels in a two-dimensional matrix form, to have a display resolution on the pixel region conforming to a VGA rating, wherein the off transition time on the drain line is 10 nanoseconds or greater and 1000 nanoseconds or smaller.

4. A solid-state imaging device according to claim 3, wherein the off transition time on the drain line is 40 nanoseconds or greater and 600 nanoseconds or smaller.

5. A solid-state imaging device according to claim 4, wherein the off transition time on the drain line is 170 nanoseconds or greater.

6. A solid-state imaging device according to claim 1, wherein the off transition time on the drain line is a half of a pixel clock period or greater and off-period or smaller to the drain line.

7. A solid-state imaging device according to claim 1, wherein the transfer drive buffer includes a transistor connected at least to the transfer line, the reset drive buffer includes a transistor connected at least to the reset line, and the drain drive buffer includes a transistor connected at least to the drain line, wherein the transistor connected to the drain line has a W/L ratio (W is a gate width, L is a gate length) set in a range of 1/5 times to 1/2500 times greater than any of a W/L ratio of the transistor connected to the transfer line and a W/L ratio of the transistor connected to the reset line.

8. A solid-state imaging device according to claim 7, wherein the transistor connected to the drain line has a W/L ratio set in a range of 1/10 times to 1/500 times greater than any of a W/L ratio of the transistor connected to the transfer

line and a W/L ratio of the transistor connected to the reset line.

9. A solid-state imaging device according to claim 1, further comprising a resistance element for limiting a drive current provided between an off-side reference line of the drain drive buffer and a reference power source regulating an off voltage to the drain line.

10. A solid-state imaging device according to claim 1, further comprising a current source for regulating a drive current provided between an off-side reference line of the drain drive buffer and a reference power source regulating an off voltage to the drain line.

11. A solid-state imaging device comprising:

unit pixels including as constituent elements

a charge generating section for generating a signal charge in an amount corresponding to a light received,

a charge storing part for storing a charge generated by the charge generating section,

a transfer gate section arranged between the charge generating section and the charge storing part and for transferring the signal charge generated by the charge generating section to the charge storing part,

a pixel signal generating section for generating a pixel signal commensurate with the signal charge stored at the charge storing part, and

a reset section for resetting the signal charge at the charge storing part;

a signal line provided for receiving the pixel signal generated by the pixel signal generating section and connected commonly with other unit pixels;

a pixel select operation, for outputting the pixel signal generated by the pixel signal generating section onto the signal line, being carried out under potential control at the charge storing part;

a drain line provided connected commonly with other unit pixels and connected to the reset section and the pixel signal generating section; and

an off voltage to be supplied to the transfer gate section having a voltage value reverse in polarity to an on voltage to be supplied to the transfer gate section, with respect to a master reference voltage regulating a reference voltage for an entire of the unit pixels.

12. A solid-state imaging device according to claim 11, incorporating a voltage generating circuit for generating the off voltage.

13. A solid-state imaging device according to claim 11, wherein the off voltage is a voltage having a difference of greater than 0.7 V from a master voltage regulating a reference voltage for an entire of the unit pixels and a magnitude in a range not to cause breakdown in the unit pixel.

14. A solid-state imaging device according to claim 13, wherein the unit pixels are structured on a well formed of a semiconductor, the off voltage being a voltage in a magnitude capable of generating a channel at an interface of the semiconductor structuring the unit pixels.

15. A solid-state imaging device comprising:

unit pixels including as constituent elements

a charge generating section for generating a signal charge in an amount corresponding to a light received,

a charge storing part for storing a charge generated by the charge generating section,

a transfer gate section arranged between the charge generating section and the charge storing part and for transferring the signal charge generated by the charge generating section to the charge storing part,

a pixel signal generating section for generating a pixel signal commensurate with the signal charge stored at the charge storing part, and

a reset section for resetting the signal charge at the charge storing part;

a signal line provided for receiving the pixel signal generated by the pixel signal generating section and connected commonly with other unit pixels;

a pixel select operation, for outputting the pixel signal generated by the pixel signal generating section onto

the signal line, being carried out under potential control at the charge storing part;

the unit pixels being structured on the well formed of a semiconductor, and further a bias line provided for fixing the well potential.

16. A solid-state imaging device according to claim 15, wherein a contact connecting between the bias line and the well is provided in each unit pixel.

17. A solid-state imaging device comprising:

unit pixels including as constituent elements

a charge generating section for generating a signal charge in an amount corresponding to a light received,

a charge storing part for storing a charge generated by the charge generating section,

a transfer gate section arranged between the charge generating section and the charge storing part and for transferring the signal charge generated by the charge generating section to the charge storing part,

a pixel signal generating section for generating a pixel signal commensurate with the signal charge stored at the charge storing part, and

a reset section for resetting the signal charge at the charge storing part and structured by a depression-type transistor;

a signal line provided for receiving the pixel signal

generated by the pixel signal generating section and connected commonly with other unit pixels; and

a pixel select operation, for outputting the pixel signal generated by the pixel signal generating section onto the signal line, being carried out under potential control at the charge storing part.

18. A solid-state imaging device according to claim 17, further comprising a drain line connected commonly with other unit pixels and connected to the reset section and the pixel signal generating section, the transistor of the reset section, in an on state, being capable of setting the charge storing part at a voltage level of the drain line upon turned on.

19. A solid-state imaging device comprising:

unit pixels including as constituent elements

a charge generating section for generating a signal charge in an amount corresponding to a light received,

a charge storing part for storing a charge generated by the charge generating section,

a transfer gate section arranged between the charge generating section and the charge storing part and for transferring the signal charge generated by the charge generating section to the charge storing part,

a pixel signal generating section for generating a pixel signal commensurate with the signal charge stored at the charge storing part, and

a reset section for resetting the signal charge at the charge storing part;

a transfer line connected commonly with other unit pixels and connected to the transfer gate section;

a transfer drive buffer for driving the transfer line;

a reset line connected commonly with other unit pixels and connected to the reset section;

a reset drive buffer for driving the reset line;

a drain line connected commonly with other unit pixels and connected to the reset section and the pixel signal generating section;

a drain drive buffer for driving the drain line; and

a signal line for receiving the pixel signal generated by the pixel signal generating section and connected commonly with other unit pixels;

whereby a pixel select operation, for outputting the pixel signal generated by the pixel signal generating section onto the signal line, is carried out under potential control at the charge storing part; and

an off transition time, on a voltage waveform on the drain line to be driven by the drain drive buffer of upon applying a drive pulse to the drain drive buffer, is given longer than an off transition time on any of the reset line to be driven by the reset drive buffer and the transfer line to be driven by the transfer driven buffer.

20. A solid-state imaging device comprising:

a solid-state imaging element having

unit pixels including, as constituent elements,

a charge generating section for generating a signal charge in an amount corresponding to a light received,

a charge storing part for storing a charge generated by the charge generating section,

a transfer gate section arranged between the charge generating section and the charge storing part and for transferring the signal charge generated by the charge generating section to the charge storing part,

a pixel signal generating section for generating a pixel signal commensurate with the signal charge stored at the charge storing part, and

a reset section for resetting the signal charge at the charge storing part;

a transfer line connected commonly with other unit pixels and connected to the transfer gate section;

a reset line connected commonly with other unit pixels and connected to the reset section;

a drain line connected commonly with other unit pixels and connected to the reset section and the pixel signal generating section; and

a signal line for receiving the pixel signal generated by the pixel signal generating section and connected commonly

with other unit pixels;

whereby a pixel select operation, for outputting the pixel signal generated by the pixel signal generating section onto the signal line, is carried out under potential control at the charge storing part; and

a waveform shaping section for receiving a drive pulse for driving the drain line and carrying out a waveform shaping such that an off transition time, on a voltage waveform in driving the drain line, is given longer than an off transition time on a voltage waveform in driving any of the reset line and the transfer line.

21. A solid-state imaging device according to claim 20, wherein the waveform shaping section carries out a waveform shaping such that an off transition time on a voltage waveform in driving the drain line is five times or greater and ten thousand times or smaller than the off transition time on both the reset line and the transfer line.

22. A drive control method for a solid-state imaging device comprising:

unit pixels including, as constituent elements,

a charge generating section for generating a signal charge in an amount corresponding to a light received,

a charge storing part for storing a charge generated by the charge generating section,

a transfer gate section arranged between the charge

generating section and the charge storing part and for transferring the signal charge generated by the charge generating section to the charge storing part,

a pixel signal generating section for generating a pixel signal commensurate with the signal charge stored at the charge storing part, and

a reset section for resetting the signal charge at the charge storing part,

a transfer line connected commonly with other unit pixels and connected to the transfer gate section;

a reset line connected commonly with other unit pixels and connected to the reset section,

a drain line connected commonly with other unit pixels and connected to the reset section and the pixel signal generating section, and

a signal line for receiving the pixel signal generated by the pixel signal generating section and connected commonly with other unit pixels,

whereby a pixel select operation, for outputting the pixel signal generated by the pixel signal generating section onto the signal line, is carried out under potential control at the charge storing part, the drive control method characterized in that:

the drain line is driven such that an off transition time, on a voltage waveform in driving the drain line, is given

longer than an off transition time on a voltage waveform in driving any of the reset line and the transfer line.

23. A drive control method according to claim 22, wherein the drain line is driven such that an off transition time on a voltage waveform in driving the drain line is five times or greater and ten thousand times or smaller than the off transition time on both the reset line and the transfer line.

24. A solid-state imaging device comprising:

an imaging region arranged with a plurality of pixels; and

a circuit region for supplying a drive pulse to the imaging region;

the pixel having

a photoelectric converting section for generating a charge commensurate with an amount of incident light,

a charge storing part for storing a charge read from the photoelectric converting section by a transfer gate section, and

a reset section for resetting the charge stored at the charge storing part;

wherein the transfer gate is connected with a transfer line, the reset section is connected with a reset line and the charge storing part is connected with a drain line through the reset section;

the circuit region supplying a first pulse toward the drain line, a second pulse toward the reset line and a third pulse toward the transfer line;

the first pulse having a waveform longer in off transition time than a waveform of the second pulse and third pulse.